WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a semiconductor chip having a top principal surface, said semiconductor chip carrying a plurality of bump electrodes on said top principal surface;

a resin layer covering said top principal surface of said semiconductor chip so as to seal said semiconductor chip,

said semiconductor chip and said resin layer thereby forming a composite semiconductor structure defined by a side wall having a plurality of corners, and

a chamfer surface formed in said side wall of said composite semiconductor structure as a part of said side wall such that said chamfer surface extends over said semiconductor chip and said resin layer.

2. A semiconductor device as claimed in claim 1, wherein said chamfer surface surrounds a top edge of said composite structure continuously, said top edge defining a top surface of said composite structure including a top surface of said resin layer.

3. A semiconductor device as claimed in claim 1, wherein said chamfer surface is formed on a top edge of said semiconductor structure in correspondence to each of said plurality of corners,

said top edge defining a top surface of said composite structure including a top surface of said resin layer.

4. A semiconductor device as claimed in claim 1, wherein said composite structure carries another chamfer surface on a bottom edge of said composite structure as a part of said side wall of said composite structure, said bottom edge defining a bottom surface of said composite structure.

5. A semiconductor device as claimed in claim 4, wherein said another chamfer surface extends along said bottom edge continuously so as to surround said composite structure laterally.

6. A semiconductor device as claimed in claim 4, further comprising another resin layer on a bottom principal surface of said semiconductor chip, said another resin layer thereby forming a part of said composite structure, said another chamfer surface being formed on said semiconductor chip and said another resin layer continuously.

7. A semiconductor device as claimed in claim 6, wherein said another chamfer surface is

formed along a bottom edge of said composite structure continuously so as to surround said composite structure laterally, said bottom edge defining a bottom surface of said composite structure.

8. A semiconductor device as claimed in claim 1, wherein said semiconductor chip carries another resin layer on a bottom principal surface thereof.

9. A semiconductor device as claimed in claim 1, wherein said chamfer surface is provided on each of said plurality of corners of said composite structure such that said chamfer surface extends substantially perpendicularly to said top principal surface of said semiconductor chip.

10. A semiconductor device as claimed in claim 2, further including another chamfer surface provided on each of said plurality of corners of said composite structure such that said another chamfer surface extends substantially perpendicularly to said top principal surface of said semiconductor chip.

11. A semiconductor device as claimed in

claim 5, further including an additional chamfer surface on each of said plurality of corners of said composite structure such that said additional chamfer surface extends substantially perpendicularly to said top surface of said semiconductor chip.

12. A semiconductor device as claimed in claim 7, further including an additional chamfer surface on each of said plurality of corners of said composite structure such that said additional chamfer surface extends substantially perpendicularly to said top surface of said semiconductor chip.

13. A semiconductor device as claimed in claim 2, wherein said resin layer has a surrounding side wall inside said chamfer surface such that said surrounding side wall is substantially perpendicularly to said top principal surface of said semiconductor chip.

14. A semiconductor device, comprising:

a semiconductor chip having a top principal surface, said semiconductor chip carrying a plurality of bump electrodes on said top principal surface;

a resin layer covering said top principal surface of said semiconductor chip so as to seal said semiconductor chip,

said semiconductor chip and said resin layer

thereby forming a composite semiconductor structure defined by a side wall having a plurality of corners, and

a step surface formed in said resin layer along said side wall of said composite structure.

15. A semiconductor device as claimed in claim 14, wherein said step surface surrounds a top edge of said composite structure continuously, said top edge defining a top surface of said composite structure including a top surface of said resin layer.

16. A semiconductor device as claimed in claim 14, wherein said step surface is formed on a top edge of said semiconductor structure in correspondence to each of said plurality of corners, said top edge defining a top surface of said composite structure including a top surface of said resin layer.

17. A semiconductor device as claimed in claim 14, wherein said composite structure carries another resin layer on a bottom edge of said composite structure as a part of said side wall of said composite structure.

18. A semiconductor device as claimed in claim 17, further comprising another step surface in said another resin layer along bottom edge of said composite structure, said bottom edge defining a bottom surface of said composite structure including a bottom surface of said another resin layer.

19. A semiconductor device as claimed in claim 18, wherein said another step surface is formed in said another resin layer continuously so as to surround said composite structure.

20. A semiconductor device as claimed in claim 15, further comprising a chamfer surface provided on each of said plurality of corners of said composite structure such that said chamfer surface extends substantially perpendicularly to said top principal surface of said semiconductor chip.

21. A semiconductor device as claimed in claim 19, further including a chamfer surface provided on each of said plurality of corners of said composite structure such that said chamfer surface extends substantially perpendicularly to said top principal surface of said semiconductor chip.

22. A semiconductor device as claimed in claim 20, further including another chamfer surface on said bottom edge of said composite structure such that said another chamfer surface surrounds said composite structure laterally, said bottom edge defining a bottom surface of said composite structure including a bottom surface of said semiconductor chip.

23. A semiconductor device as claimed in claim 15, further including a chamfer surface on said bottom edge of said composite structure such that said chamfer surface surrounds said composite structure laterally, said bottom edge defining a bottom surface of said composite structure including a bottom surface of said semiconductor chip.

24. A semiconductor device, comprising:

a semiconductor chip having a top principal surface, said semiconductor chip carrying a plurality of bump electrodes on said top principal surface;

a resin layer covering said top principal surface of said semiconductor chip so as to seal said semiconductor chip,

a chamfer surface formed in a side wall of said semiconductor chip as a part of said side wall such that said chamfer surface surrounds said semiconductor chip along a top edge thereof,

said resin layer covering said chamfer surface.

25. A semiconductor device as claimed in claim 24, further including: another chamfer surface formed in said side wall of said semiconductor chip as a part of said side wall such that said chamfer surface surrounds said semiconductor chip along a bottom edge thereof, said bottom edge defining a bottom surface of said semiconductor chip, and another resin layer provided on said bottom surface of said semiconductor chip so as to cover said another chamfer surface.

26. A method of fabricating a semiconductor device, comprising the steps of:

forming a resin layer on a principal surface of a semiconductor substrate;

grooving said resin layer along a dicing line on said semiconductor substrate to form a V-shaped groove having a substantially V-shaped cross-section such that said V-shaped groove reaches said semiconductor substrate; and

dicing, after said step of grooving, said semiconductor substrate along said V-shaped groove by forming a dicing groove with a width smaller than a width of said V-shaped groove.

27. A method as claimed in claim 26, wherein said step of grooving is conducted along said dicing line for an entire length thereof on said substrate.

28. A method as claimed in claim 26, wherein said step of grooving is conducted in the vicinity of cross points of mutually crossing dicing lines to form said V-shaped groove in the form of isolated cross-mark patterns.

29. A method as claimed in claim 35, wherein said step of grooving is conducted by a saw blade having a V-shaped saw blade edge between a pair of mutually parallel lateral surfaces, with such a depth that said V-shaped groove formed by said V-shaped saw blade has a pair of lateral surfaces extending substantially perpendicularly to a principal surface of said semiconductor substrate in continuation to a V-shaped bottom of said V-shaped groove, and such that said lateral surfaces of said saw blade engage said side walls of said V-shaped groove.

30. A method as claimed in claim 26, further comprising, after said step of forming said resin layer but before said step of grooving said resin layer, the step of reducing a thickness of said semiconductor substrate by grinding a rear surface of said semiconductor substrate.

31. A method of fabricating a semiconductor device, comprising the steps of:

forming a resin layer on a principal surface of a semiconductor substrate;

dicing said semiconductor substrate along a dicing line by forming a dicing groove through said resin layer and through said semiconductor substrate; and

grooving, after said step of dicing of said semiconductor substrate, said resin layer along said dicing line to form a V-shaped groove having a substantially V-shaped cross-section in said resin layer such that said V-shaped groove has a width larger than a width of said dicing groove and reaches said semiconductor substrate.

32. A method as claimed in claim 31, wherein said step of grooving is conducted along said dicing line for an entire length thereof on said substrate.

33. A method as claimed in claim 31, wherein said step of grooving is conducted in the vicinity of cross points of mutually crossing dicing lines to form said V-shaped groove in the form of isolated cross-mark patterns.

34. A method as claimed in claim 31, wherein said semiconductor substrate is mounted on a dicing apparatus by an adhesive tape.

35. A method as claimed in claim 31, further comprising, after said step of forming said resin layer but before said step of grooving, the step of reducing a thickness of said substrate.

36. A method of fabricating a semiconductor device, comprising the steps of:

forming a resin layer on a principal surface of a semiconductor substrate;

grooving said resin layer along a dicing line on said semiconductor substrate to form a first groove having a substantially rectangular cross-section and a first width in said resin layer; and

dicing, after said step of grooving, said semiconductor substrate along said first groove by forming a second groove with a second width smaller than said first width of said first groove.

37. A method as claimed in claim 36, wherein said step of grooving is conducted along said dicing line for an entire length thereof on said substrate.

38. A method as claimed in claim 36, wherein said step of grooving is conducted in the vicinity of cross points of mutually crossing dicing lines to form said first groove in the form of isolated cross-mark patterns.

39. A method of fabricating a semiconductor device, comprising the step of:

adhering a semiconductor substrate on a dicing apparatus by an adhesive tape;

dicing said semiconductor substrate in a first direction such that said adhesive tape remains substantially intact;

dicing said semiconductor substrate in a second, different direction together with said adhesive tape, to form a plurality of adhesive strips each carrying thereon a plurality of semiconductor chips aligned in a row; and

applying a V-shaped saw blade having a V-shaped saw edge laterally to each of said adhesive strips such that said V-shaped saw blade cuts into a gap formed between a pair of adjacent semiconductor chips by said dicing step conducted in said first direction, said saw blade thereby forming a chamfer surface on a side wall of said semiconductor chips such that said chamfer surface extends, in each of said semiconductor chips, generally perpendicularly to a principal surface of said semiconductor chip.

40. A method of fabricating a semiconductor device, comprising the steps of:

forming a V-shaped groove on a top surface of a semiconductor substrate, said semiconductor device carrying an electronic circuit on said top surface;

forming a resin layer on said top surface of said semiconductor substrate so as to fill said V-shaped groove; and

dicing said semiconductor substrate by a dicing saw having a blade width smaller than a width

of said V-shaped groove, along said V-shaped groove.

41. A method as claimed in claim 40, wherein said method further comprises the steps of: forming another V-shaped groove on a bottom surface of said semiconductor substrate; and forming another resin layer on said bottom surface of said semiconductor substrate so as to fill said another V-shaped groove, and

wherein said dicing step is conducted by said dicing saw such that said dicing saw cuts said resin layer and said another resin layer simultaneously.

42. A method of fabricating a semiconductor device, comprising the steps of:

slicing a semiconductor substrate from a semiconductor ingot;

applying a resin layer on a first surface of said semiconductor substrate such that said resin layer has a planarized surface;

grinding a second surface of said semiconductor substrate while using said planarized surface of said resin layer as a reference surface, to form a planarized surface on said second surface; and

grinding said first surface while using said second, planarized surface as a reference surface, to form a planarized surface on said first surface.

43. A transportation device of a semiconductor device, comprising:

a tray member adapted to support a semiconductor device in a face-down state, said semiconductor device carrying a plurality of bump electrodes thereon, said tray member having an opening for accommodating said bump electrodes when said semiconductor device is mounted on said tray member; and

a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said semiconductor device is mounted on said tray member,

wherein said tray member includes a chamfer surface for engagement with a corresponding chamfer surface formed on said semiconductor device.

44. A transportation device as claimed in claim 43, wherein said chamfer surface of said tray member is formed so as to surround said opening continuously.

45. A transportation device as claimed in claim 43, wherein said chamfer surface of said tray member is formed on four corners of said opening.

46. A transportation device of a semiconductor device, comprising:

a tray member adapted to support a semiconductor device in a face-down state, said semiconductor device carrying a plurality of bump electrodes thereon, said tray member having an opening for accommodating said bump electrodes when said semiconductor device is mounted on said tray member; and

a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said semiconductor device is mounted on said tray member,

wherein said tray member includes a step surface for engagement with a corresponding step surface formed on said semiconductor device.

47. A transportation device as claimed in claim 46, wherein said step surface of said tray member is formed so as to surround said opening continuously.

48. A transportation device as claimed in claim 46, wherein said step surface of said tray member is formed on four corners of said opening.

49. A method of fabricating a semiconductor device, comprising the steps of:

mounting a semiconductor device having a chamfered surface and a plurality of bump electrodes

on a transportation device,

said transportation device comprising a tray member adapted to support said semiconductor device in a face-down state, said tray member having an opening for accommodating said bump electrodes when said semiconductor device is mounted on said tray member, and a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said semiconductor device is mounted on said tray member, said tray member including a chamfer surface for engagement with said chamfer surface on said semiconductor device; and

transporting said semiconductor device in a state mounted on said transportation device.

50. A method of fabricating a semiconductor device, comprising the steps of:

mounting a semiconductor device having a stepped surface and a plurality of bump electrodes on a transportation device,

said transportation device comprising a tray member adapted to support said semiconductor device in a face-down state, said tray member having an opening for accommodating said bump electrodes when said semiconductor device is mounted on said tray member, and a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said semiconductor device is mounted on said tray member, said tray member including a stepped surface for engagement with said stepped surface on said semiconductor device; and

transporting said semiconductor device in a

state mounted on said transportation device.